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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,994	06/09/2005	Keiichi Murakami	2005-0873A	1367

513 7590 05/15/2006

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/537,994	MURAKAMI, KEIICHI	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-15 and 17* is/are allowed.

6)☒ Claim(s) *1-10 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/05-09/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

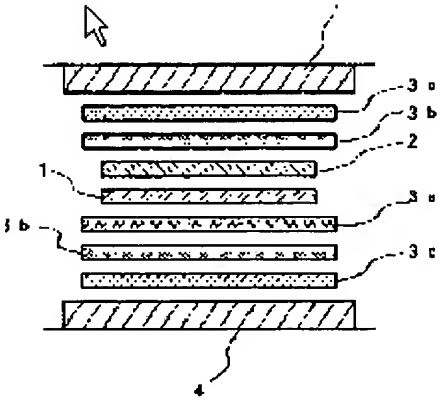
Claim Rejections - 35 USC § 103

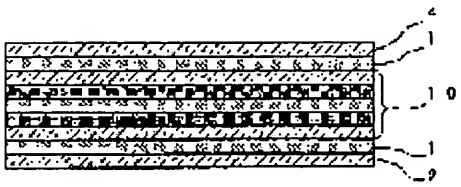
1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsurayama, Japanese Patent Abstract 10-242621 in view of Nakamura et al., U.S. Patent 6,739,040 B1.

3. Katsurayama discloses a semiconductor process substantially as claimed. See Drawings 2 and 10(f) where Katsurayama teaches the following limitations.





4. Pertaining to claim 1, Katsurayama discloses a method for manufacturing a flat printed wiring board in which spaces between circuit patterns are filled with a resin, said method comprising the following steps:

laminating via a mold release film (see paragraph 0026) a plurality of sets of laminated bodies formed by superposing a semi-cured resin sheet on a printed wiring board with said circuit patterns formed thereon;

placing the laminated plural sets of said laminated bodies interposed between a pair of smoothing plates; and

curing said resin and then

polishing said cured resin covering said circuit patterns, thereby exposing said circuit patterns (see paragraph 0045). However, Katsurayama fails to teach collectively pressing said laminated bodies in a reduced pressure atmosphere. Nakamura teaches fabricating a multilayered printed wiring board by collectively pressing said laminated bodies in a reduced pressure atmosphere. In view of Nakamura, it would have been obvious to one of ordinary skill in the art to incorporate pressing laminated bodies in a reduced pressure atmosphere because the resin composition layer side thereof by pressurizing and heating under a vacuum condition (column 4, lines 53-55).

5. Pertaining to claim 2, Katsurayama teaches the method for manufacturing the flat wiring board according to claim 1, wherein said circuit patterns are formed on both sides of said printed wiring board (see drawing 10(a)-10(f).

6. Pertaining to claim 3, Katsurayama teaches the method for manufacturing the flat wiring board according to claim 2, including a further step of superposing metallic foil with a roughened surface facing said resin layer onto said resin layer.

7. Pertaining to claim 4, Katsurayama teaches the method for manufacturing the flat wiring ward according to claim 3, wherein said metallic foil is formed with a different kind of metal than the kind of metal used to form said circuit pattern.

8. Pertaining to claim 5, Katsurayama teaches the method for manufacturing the flat printed wiring board according to claim 4, wherein said metallic foil is nickel (because Katsurayama teaches the use of nickel, it is well known that nickel and copper are used in printed circuit boards, this is merely nothing more than the substitution of parts).

9. Pertaining to claim 6, Katsurayama teaches the method for manufacturing the flat printed wiring board according to claim 3 wherein the step of polishing comprises the steps of:
ceramic buff polishing to remove resin layers from the circuit pattern; and
finish polishing to reduce the average roughness of the surface of the flat printed wiring board (see paragraph 0045 of Katsurayama and column 6, lines 22-23 of Nakamura).

10. Pertaining to claim 7, the combined teachings discloses the method for manufacturing the flat printed wiring board according to claim 1 wherein said circuit patterns are formed by an additive method.

11. Pertaining to claim 8, Katsurayama teaches a method for manufacturing a flat printed wiring board in which spaces between circuit patterns are filled with a resin, said method comprising the following steps:

superposing a semi-cured resin sheet on said circuit pattern printed on a printed wiring board to form a board assembly;

stacking a predetermined number of said board assemblies with a mold release film interposed between every adjacent said board assembly to create a stack of board assemblies;

superposing a first smoothing plate on a first surface of said stack of board assemblies via a first mold release film;

superposing a second smoothing plate on a second surface of said stack of board assemblies via a second mold release film;

heating said stack of board assemblies so as to cure the semi-cured resin sheets;

polishing each board assembly so as to expose each corresponding said circuit pattern. However, Katsurayama fails to teach pressing said first and second smoothing plates and said stack of board assemblies in a reduced atmosphere environment. Nakamura teaches fabricating a multilayered printed wiring board by collectively pressing said laminated bodies in a reduced pressure atmosphere. In view of Nakamura, it would have been obvious to one of ordinary skill in the art to incorporate pressing laminated bodies in a reduced pressure atmosphere because the resin composition layer side thereof by pressurizing and heating under a vacuum condition (column 4, lines 53-55).

12. Pertaining to claim 9, Katsurayama in view of Nakamura teaches the method for manufacturing the flat printed wiring board according to claim 8, wherein said printed wiring board of said board assembly comprises a first board surface and a second board surface, and wherein said circuit pattern is printed on said first board surface, and
wherein a second circuit pattern is printed on said second board surface, and
wherein a second semi-cured resin sheet is superposed on said second circuit pattern, and
wherein each board assembly is further polished to expose each corresponding second circuit pattern.

13. Pertaining to claim 10, Katsurayama in view of Nakamura teaches the method for manufacturing the flat printed wiring board of claim 9 further comprising the steps of:
superposing a metallic foil with a roughened surface onto said semi-cured resin sheet wherein the roughened surface contacts said semi-cured resin sheet, and
superposing a second metallic foil with a second roughened surface onto said second semi-cured resin sheet wherein the second roughened surface contacts said second semi-cured resin sheet.

14. Pertaining to claim 16, Katsurayama in view of Nakamura teaches the method for manufacturing the flat printed wiring board according to claim 1, including a further step of superposing a metallic foil with a roughened surface facing said resin layer onto said resin layer (please see column 6, lines 16-23 of Nakamura).

Allowable Subject Matter

15. Claims 11-15 and 17 allowed.

16. The following is an examiner's statement of reasons for allowance: the prior art does not anticipate nor render obviousness as to removing the corresponding metallic foils after semi-curing the wiring board.

17. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC